IN THE CLAIMS

Please enter the following indicated amendments.

1– 7. (Cancelled).

8. (Previously Amended) An SEU-resistant circuit comprising

a logic gate having an input and an output;

a feedback path from the output of the logic gate to the input of the logic gate, the feedback path comprising two or more logic elements, said logic gate and said two or more logic elements each comprising an input to output pulse response operable for delaying a propagation time of a pulse propagating therethrough and for selectively reducing a pulse width thereof; and

the logic gate and the two or more logic elements being operable for reducing in size an instance of a potentially SEU producing glitch introduced at the input of the logic gate before the potentially SEU producing glitch propagates through the feedback path to the input of the logic gate, the input to output pulse response of the logic gate and the two or more logic elements being substantially similar in that the resulting amount of pulse propagation delay and amount of reduction of the pulse width of the potentially SEU producing glitch is spread substantially evenly among the logic gate and the two or more logic elements.

9. (Cancelled).

10. (Previously Amended) The SEU-resistant circuit of claim 8 wherein the input to output pulse response of the logic elements is balanced such that a rise time and fall time of the input to output pulse response is approximately the same for each of the logic elements.

11. (Currently Amended) The SEU-resistant circuit of claim 8 <u>wherein said two or more logic elements</u> further ~~comprising~~ <u>comprise</u> a plurality of logic gates, an input to output pulse response of the plurality of logic gates and the two or more logic elements being configured to produce a pulse propagation delay approximately no longer than a maximum pulse propagation delay of the slowest of the plurality of logic gates when the slowest logic gate is fully loaded with maximum fan out.

12. (Previously Amended) The SEU-resistant circuit of claim 11 wherein the input to output pulse response of the plurality of logic gates and each of the two or more logic elements is operable to prevent a glitch with a time length less than approximately one-half of the maximum pulse propagation delay from passing through the plurality of logic gates or through each of the two or more logic elements without being reduced in size such that said glitch is unable to trigger a subsequent logic element .

13. (Previously Amended) The SEU-resistant circuit of claim 11 wherein the input to output pulse response of the plurality of logic gates and the two or more logic elements does not substantially reduce the time length of a pulse with a time length greater than two times the maximum pulse propagation delay.

14. (Withdrawn) An SEU-resistant circuit having a first state and a second state, the SEU-resistant circuit comprising

a first flip-flop having a first state and a second state, the first flip-flop configured to change state upon application of a signal to a first flip-flop signal input;

a second flip-flop having a first state and a second state equivalent to the first state and the second state of the first flip-flop, the second flip-flop configured to change state upon application of a signal to a second flip-flop signal input;

the first flip-flop being coupled to the second flip-flop such that the SEU-resistant circuit does not change from its first state to its second state unless the state of the first flip-flop agrees with the state of the second flip-flop;

an input to receive a signal to cause the SEU-resistant circuit to change states when the signal changes states;

the input coupled to the first flip-flop signal input;

the input coupled to the second flip-flop signal input through a delay circuit; and

the input is for one of a clock, reset or preset signal.

15. (Withdrawn) The SEU-resistant circuit of claim 14, wherein the delay circuit is non-inverting.

16. (Withdrawn) The SEU-resistant circuit of claim 14, wherein the delay circuit has a delay greater than the maximum expected glitch time.

17— 21. (Cancelled).

22. (Withdrawn) An SEU-resistant flip-flop comprising

a Data input;

a GB input;

a network responsive to signals applied to the Data input and the GB input;

the network having a Q1 output which has the value of the signal applied to the Data input when the signal applied to the GB input is low;

the network having a Q2 output which has the value of the signal applied to the Data input D seconds after the signal applied to the GB input is low;

the Q1 output of the network being coupled to a Q1 node;

the Q2 output of the network being coupled to a Q2 node;

a two-input one-output TAG, the output of the TAG being configured to change state only if the value of the signal on its first input is the same as the value of the signal on its second input;

the first input of the TAG being coupled to the Q1 node;

the second input of the TAG being coupled to the Q2 node;

the output of the TAG being coupled to a QB node;

a first slow inverter having its input coupled to the QB node and its output coupled to the Q1 node; and

a second slow inverter having its input coupled to the QB node and its output coupled to the Q1 node.

23. (Withdrawn) The SEU-resistant flip-flop of claim 22 further comprising

a transmission gate, gated by the value of the signal in the GB node, in a signal path between the first slow inverter and the Q1 node; and

a transmission gate, gated by the value of the signal on the GB node, in a signal path between the second slow inverter and the Q2 node.

24. (Withdrawn) The SEU-resistant flip-flop of claim 22 further comprising an inverter coupled to the QB node.

25. (Withdrawn) The SEU-resistant flip-flop of claim 22 wherein the TAG comprises

two series-connected P-type FETs, the gate of a first P-type FET coupled to the Q1 node, the gate of a second P-type FET coupled to the Q2 node, the series-connected P-type FETs having a supply end and a connection end;

two series-connected N-type FETs, the gate of a first N-type FET coupled to the Q1 node, the gate of a second N-type FET coupled to the Q2 node, the series-connected N-type FETs having a ground end and a connection end; and

the connection end of the series-connected N-type FETs being coupled to the connection end of the series-connected P-type FETs and to the QB node.

26. (Withdrawn) The SEU-resistant flip-flop of claim 25 wherein

the P-type FET coupled to the Q2 node is at the connection end of the series-connected P-type FETs; and

the N-type FET coupled to the Q2 node is at the connection end of the series-connected N-type FETs.

27. (Withdrawn) The SEU-resistant flip-flop of claim 22 wherein the network comprises

a first inverter having its input coupled to the GB input, the output of the first inverter being coupled to a G node;

a delay G having its input coupled to the G node, the output of the delay G being coupled to a G2 node;

an inverter having its input coupled to the G2 node and its output coupled to a GB2 node;

a first transmission gate coupled between the Data input and the Q1 node and gated by the signals on the GB and G nodes; and

a second transmission gate coupled between the Data input and the Q2 node and gated by the signals on the GB2 and G2 nodes.

28. (Withdrawn) The SEU-resistant flip-flop of claim 27 wherein the delay G comprises a first delay coupled in series with a second delay.

29. (Withdrawn) The SEU-resistant flip-flop of claim 27 further comprising a buffer coupled between the Data input and the first and second transmission gates.

30. (Currently Amended) A method for reducing the vulnerability of an electronic circuit to single event upsets, comprising:

providing one or more logic gates for said circuit with a feedback path from an output of a respective of the one or more logic gates to an input thereof;

inserting one or more logic elements into the feedback path; and

providing that the one or more logic ~~circuits~~ elements and the one or more logic gates each have an input to output pulse response such that an initial input glitch with a pulse width less than a pulse width L1 effectively does not pass through a respective of the one or more logic ~~circuits~~ elements or a respective of the one or more logic gates because a resulting diminished output glitch is not capable of triggering a change of state of ~~a subsequent logic element~~ said respective of the one or more logic elements or said respective of the one or more logic gates; and

providing that if the initial input glitch has a pulse width greater than pulse width L1 but less than a pulse width L2 then the resulting diminished output glitch effectively passes through the respective of the one or more logic ~~circuits~~ elements or the respective of the one or more logic gates because the resulting output glitch is then capable of triggering a change of state of ~~the subsequent logic device~~ said respective of the one or more logic elements or said respective of the one or more logic gates but that the resulting diminished output glitch then has a reduced pulse width as compared to the initial input glitch; and

providing that the pulse width L1 and the pulse width L2 are approximately equal for the respective of the one or more logic ~~circuits~~ elements and for the respective of the one or more logic gates.

31. (Currently Amended) The method of claim 30 wherein the one or more logic gates comprise a first FET comprising a first channel and a second FET comprising a second channel, ~~wherein said providing step comprises~~ further comprising:

adjusting the characteristics of the first channel of the first FET.

32. (Previously Amended) The method of claim 31 wherein said step of adjusting comprises changing at least one of a width or a length of the first channel of the first FET.

33. (Previously Amended) The method of claim 32 wherein said step of changing comprises making the first channel wider.

34. (Previously Amended) The method of claim 31 wherein said step of adjusting comprises inserting a non-linearity into the first channel.

35. (Previously Amended) The method of claim 34 wherein the non-linearity is a right angle.

36. (Previously Amended) The method of claim 31 wherein an input signal pulse having a signal pulse width greater than a pulse width L3 effectively passes through the respective one or more logic gates or passes through the respective one or more logic ~~circuits~~ elements without a substantial change in a resulting output signal pulse width.

37. (Previously Amended) The method of claim 31 further comprising:

providing that said one or more logic gates and the one or more logic ~~circuits~~ elements comprises a latch ~~circuit~~ element.